In the Specification:

Page 4, paragraph 2, lines 9-30 should read as follows:

More particularly, the level-shifting section 12 includes an input transistor N_1 having a control, here gate, electrode coupled to a +2.1 volt supply, a first electrode coupled to the input logic signal IN, and a second electrode. An output pair of serially coupled complementary type transistors, i.e., P type MOSFET P_2 and N type MOSFET N_2, is provided. A first one of the pair of transistors P_2 has a first electrode coupled to a source, not shown, of the third voltage level (+2.5 volts) through a first switching transistor P type MOSFET P_3 and a control electrode coupled to the second electrode of the input transistor N_1. A junction 16 between the output pair of transistors P_2 , N_2 provides the output terminal OUT for the level-shifting circuitry 10. A control electrode of the second one of the pair of transistors N_2 is connected to the first electrode of the input transistor N_1. The second one of the pair of transistors N_2 has a second electrode coupled to the second voltage level, here ground, through a second switching transistor N_3. The first and second switching transistors P-type MOSFET P_3 and N-Type MOSFET N_3 are fed by the enable/disable signal ENABLE, the transistor P_3 being coupled to the enable/disable signal ENABLE via an inverter 18, as shown. The level-shifting section 12 includes an additional transistor P type MOSFET P_1. The additional transistor P_1 has a control electrode connected to the junction 16, a first electrode coupled to the source of the third voltage level +2.5 through the first switching transistor P_3 and a second electrode connected to the second electrode of the input transistor N_1. The input transistor N_1 and the additional transistor P_1 are of opposite conductivity type. The enable/disable circuit 14 includes an inverter 18 fed by the enable/disable signal ENABLE. The inverter 18 having an output coupled to the control electrode of the first switching transistor P_3.